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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/625,174	07/22/2003	Hyun-Jin Chung	51876P351	8246
8791	7590	11/17/2004	EXAMINER	
BLAKELY SOKOLOFF TAYLOR & ZAFMAN 12400 WILSHIRE BOULEVARD SEVENTH FLOOR LOS ANGELES, CA 90025-1030			THOMAS, ERIC W	
			ART UNIT	PAPER NUMBER
			2831	

DATE MAILED: 11/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/625,174

Applicant(s)

CHUNG, HYUN-JIN

Examiner

Eric W Thomas

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 26 August 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1 and 3-10 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1 and 3-10 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 22 July 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

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**INTRODUCTION**

The examiner acknowledges, as recommended in the MPEP, the applicant's submission of the amendment dated 8/26/04. At this point, claims 1, 5, 6 have been amended; and claim 2 has been cancelled. Thus claims 1, 3-10 are pending in the instant application.

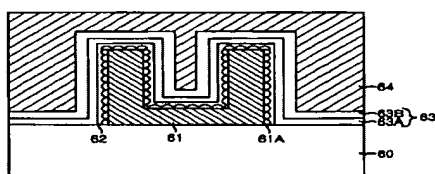
**DETAILED ACTION*****Claim Rejections - 35 USC § 103***

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

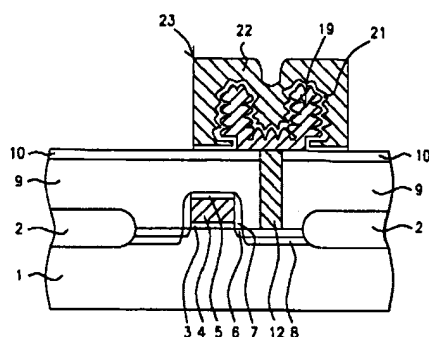
2. Claims 1, 3-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. (US 2003/0052374 A1) in view of Chang et al. (US 6,194,265).

FIG. 8



Lee et al. disclose in fig. 8, a substrate (60), a bottom electrode (61) formed on the substrate, an oxygen-diffusing layer (62) containing nitrogen (paragraph 80) on the bottom electrode, an oxygen diffusion barrier layer (63A) containing aluminum (paragraph 86) on the oxygen diffusing layer; a dielectric layer (63B) on the oxygen diffusion barrier layer; and a top electrode (64) on the dielectric layer.

Lee et al. (as shown in fig. 8) discloses the claimed invention except for an interlayer insulating layer on the substrate; a contact plug connected to the substrate by passing through the interlayer insulating layer, and the bottom electrode formed on the insulating layer and the contact plug.



Chang et al. teach (in fig. 12) the use of an interlayer-insulating layer (9) on a substrate (1); a contact plug (12) connected to the substrate by passing through the interlayer insulating layer; and the bottom electrode formed on the insulating layer and the contact plug.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the system of Lee et al. by forming the capacitor on a substrate, wherein an interlayer-insulating layer is formed on the substrate; a contact plug passes through the interlayer insulating layer connect to the substrate; and the bottom electrode is formed on the insulating layer and the contact plug, since such a modification would allow a capacitor connection to a specific area of the semiconductor substrate, which would allow for additional capacitors (and source and drain regions) to be formed on the substrate.

Regarding claim 3, Lee et al. disclose the bottom electrode includes hemispherical grains in a surface thereof.

Regarding claim 4, Lee et al. disclose the oxygen diffusion barrier layer is an alumina layer (paragraph 81).

Regarding claim 5, Lee et al. disclose a method for fabricating a capacitor, comprising the steps of:

forming a bottom electrode (61);

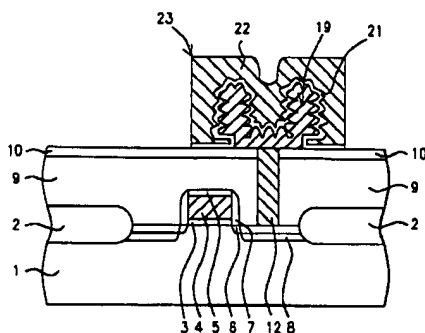
forming an oxygen diffusion layer (62) containing nitrogen (paragraph 80) on the bottom electrode.

forming an oxygen diffusion barrier layer (63A) containing aluminum on the bottom electrode;

forming a dielectric layer (63B) on the oxygen diffusion barrier layer; and

forming a top electrode (64).

Lee et al. disclose the claimed invention except for steps of forming an interlayer insulating layer on a substrate; forming a contact plug connected to the substrate by passing through the interlayer insulating layer; and forming the bottom electrode on the interlayer insulating layer and the contact plug



Chang et al. teach (in fig. 12) the method of forming an electrical system, wherein before the steps of forming the capacitor:

- a) forming an interlayer-insulating layer (9) on a substrate (1);
- b) forming a contact plug (12) connected to the substrate by passing through the interlayer insulating layer;
- and c) forming the bottom electrode formed on the insulating layer and the contact plug.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the method of forming the system of Lee et al. by

- a) forming an interlayer-insulating layer (9) on a substrate (1);
- b) forming a contact plug (12) connected to the substrate by passing through the interlayer insulating layer;
- and c) forming the bottom electrode on the insulating layer and the contact plug, since such a modification would allow a capacitor connection to a specific area on the semiconductor substrate, which would allow for additional capacitors (and source and drain regions) to be formed on the substrate.

Regarding claim 6, Lee et al. disclose step (a) includes the steps of:

- A1) forming a hemi-spherical grains (61A) on a surface of the bottom electrode;
- and

Regarding claim 7, Lee et al. disclose the oxygen diffusion barrier layer containing nitrogen is formed by using a rapid thermal process (paragraph 95).

Regarding claim 8, Lee et al. disclose the oxygen diffusion barrier is an alumina layer (see paragraph 86).

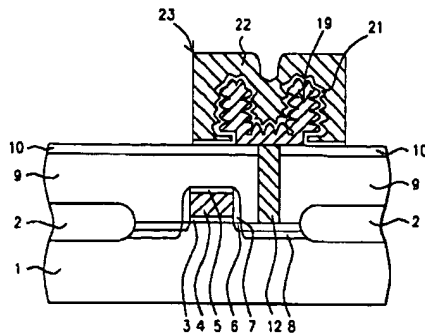
Regarding claim 9, Lee et al. disclose the alumina layer is formed from a low pressure chemical vapor technique (claim 25).

3. Claims 5, and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ahn et al. (KR 2001-63468) in view of Lee (US 6,355,519) and Chang et al. (US 6,194,265).

Regarding claim 5, Ahn et al. disclose a method for fabricating a capacitor, comprising the steps of:

- a) forming a bottom electrode (12);
- b) forming an oxygen diffusion barrier layer (13) containing aluminum on the bottom electrode;
- c) forming a dielectric layer (14) on the oxygen diffusion barrier layer; and
- d) forming a top electrode (16).

Ahn et al. disclose the claimed invention except for the steps of forming an interlayer insulating layer on a substrate; forming a contact plug connected to the substrate by passing through the interlayer insulating layer; and forming the bottom electrode on the interlayer insulating layer and the contact plug; and the step of forming an oxygen diffusion layer containing nitrogen on the bottom electrode.



Chang et al. teach (in fig. 12) the method of forming an electrical system, wherein before the steps of forming the capacitor:

- a) forming an interlayer-insulating layer (9) on a substrate (1);
- b) forming a contact plug (12) connected to the substrate by passing through the interlayer insulating layer;
- and c) forming the bottom electrode formed on the insulating layer and the contact plug.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the method of forming the system of Ahn et al. by

- a) forming an interlayer-insulating layer (9) on a substrate (1);
- b) forming a contact plug (12) connected to the substrate by passing through the interlayer insulating layer;
- and c) forming the bottom electrode on the insulating layer and the contact plug, since such a modification would allow a capacitor connection to a specific area on the semiconductor substrate, which would allow for additional capacitors (and source and drain regions) to be formed on the substrate.



Lee teaches the use of an oxygen diffusing layer containing nitrogen formed between an alumina layer and an electrode.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the capacitor of Ahn et al. by forming an oxygen diffusion layer containing nitrogen between the alumina layer and the electrode as taught by Lee, since such a modification would prevent the formation of a native oxide layer on a surface of the first electrode.

Regarding claim 8, Ahn et al. disclose the oxygen diffusion barrier is an alumina layer (see abstract).

4. Claims 9-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ahn et al. (KR 2001-63468), Lee (US 6,355,519), and Chang et al. (US 6,194,265) as applied to claim 8 above, and further in view of Ahn et al. (US 2002/0094624 A1).

Regarding claim 9, Ahn et al. disclose the claimed invention except for the alumina layer is formed by using a low pressure chemical vapor deposition technique or an atomic layer deposition technique.

Ahn et al. ('624) teaches that it is known to form an alumina layer by an atomic layer deposition technique (paragraph 17).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the alumina layer of Ahn et al. ('468) with the atomic layer deposition technique as taught by Ahn et al. ('624), since form a layer having excellent uniformity.

Regarding claim 10, Ahn et al. teach that the alumina is formed at a temperature of about 200 – 450 degrees C).

***Response to Arguments***

5. Applicant's arguments with respect to claims 1, 3-10 have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.


Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric W Thomas whose telephone number is 571-272-

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1985. The examiner can normally be reached on M,Tu,Sat 9 am - 9:30 pm; W, Th, F 6 pm -10:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dean Reichard can be reached on 571-272-1984. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

A handwritten signature in black ink, appearing to read 'C72' followed by a long horizontal stroke.

Eric W Thomas  
Examiner  
Art Unit 2831

ewt